CPRE 4920 Status Report 05

3/12/2025 – 03/26/2026

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Cache Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

  Since the last status update, we have integrated the major functional components and started firmware.

- **Past Week Accomplishments**

  - Colin McGann: Worked on integration, square root, and normal calculation
  - Jack Tonn: competition entry, core documentation
  - Dawud Benedict: Found new issue in SRAM synthesis with PDN layer. Trying to fix.
  - Michael Drobot: Core controller and submodules completed, tested, and integrated. All functionality is done (commercial SRAM, multicore, inbox/outbox, task switchover, job dispatch, etc). Worked with Colin to get vertex shading fully completed. Started firmware work, made uGPU device headers and math utilities. Edited ChipFoundry competition submission.
  - Sam Forde: com SRAM
  - Josh Arceo: Created a serializer module, integrated serialization into fragment fifo, updated unit tests
  - Emil Kosic: Successfully ran pk stream read, cleaned up code, and began an initial PR for integration

- **Pending Issues**
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- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Colin McGann	Worked on integration, square root and normal	50	400
Jack Tonn	competition entry, core documentation	15	295
Dawud Benedict	Cache synth	5	168
Michael Drobot	Core controller integration, testing, firmware	50	392
Sam Forde	Com SRAM	5	141
Josh Arceo	Serializer, serializing fifo, unit tests	30	160
Emil Kosic	Bridge improvements and PR work	15	161

- **Plans for the upcoming weeks**
  - Colin McGann: More integration, spi mem fixes, and rasterizer additions
  - Jack Tonn: Core block diagram and address coalescer
  - Dawud Benedict: Cache synth
  - Michael Drobot: frag fifo integration & demos
  - Sam Forde: com SRAM
  - Josh Arceo: Implement force_mail to fifo, finish area optimization once cache synthesis issues are resolved
  - Emil Kosic: Complete PR for bridge module and begin integration